IN THE SPECIFICATION

In compliance with 37 C.F.R. §1.177. Applicants amend the specification as follows (MPEP 1451):

At Col. 1, line 4, before the heading "CROSS REFERENCE TO RELATED APPLICATION," please insert the following section:

RELATED REISSUE APPLICATIONS

More than one reissue application has been filed for the reissue of U.S. Patent No. 6,325,294. The reissue applications are the initial reissue Application No. 10/729,584 filed December 4, 2003, a divisional reissue Application No. 11/849,941, filed September 4, 2007, a continuation reissue Application No. 11/849,868, filed September 4, 2007, and another continuation reissue Application No. 11/849,899, filed September 4, 2007, the teachings of all of which are incorporated by reference herein.

Additional amendments have been made to merely correct minor errors that were not already corrected by Certificate of Correction.

Please amend the first full paragraph in col. 3 as follows:

In a preferred embodiment of the invention, the integrated circuit receiver and transmitter are operated in a spread spectrum mode and in the frequency range of 200 MHZ ~~Mhz~~ to 10 GHz ~~GKz~~, with the range of 800 MHZ to 8 GHZ being the range of most importance. This operation has the effect of avoiding errors or improper operation due to extraneous signal sources and other sources of interference, multipathing, and reflected radiation from the

surrounding environment.

Please amend the paragraph at Col. 8, lines 27-34, as follows:

FIG. 4A through FIG. 4D are cross sectional views taken along lines [4--4] line 4A-4D of FIG. 3 showing four processing steps used in constructing the enclosed transceiver shown in FIG. 3. FIG. 4A shows in cross sectional view IC 32 bonded to base support member 30 by means of a spot or button of conductive epoxy material 56. Conductive strip 48 is shown in cross section on the upper surface of base support member 30.

Please amend the paragraph at Col. 13, lines 53-55, as follows:

Third, a single conductor in the top layer accomplishes both the first and second functions. Sec, for example, the conductor in FIG. 11 identified as areas 226, 222, and [216] 218.

CERTIFICATE OF CORRECTION

In order to incorporate those corrections made in the Certificate of Correction issued October 1, 2002, Applicants amend the specification as follows (MPEP 1411.01).

Please replace the Abstract, Item 57, on the cover sheet of the patent with the following:

The present invention teaches a method of manufacturing an enclosed transceiver, such as a radio frequency identification ("RFID") tag. Structurally, in one embodiment, the tag comprises an integrated circuit (IC) chip, and an RF antenna mounted on a thin film substrate powered by a thin film battery. A variety of antenna

geometries are compatible with the above tag construction. These include monopole antennas, dipole antennas, dual dipole antennas, a combination of dipole and loop antennas. Further, in another embodiment, the antennas are positioned either within the plant of the thin film battery or superjacent to the thin film battery.

Please replace the paragraph at Col. 2, lines 37-65, with the following:

To accomplish this purpose and object, we have invented and developed a new and improved radio frequency identification device, an associated electrical system, and a method for communicating with a remote RFID device from a local interrogator and controller. The size of this new device will typically be on the order of one inch square and 0.03 inches thick, or only slightly larger and slightly thicker than a postage stamp. This device includes, in combination, an integrated circuit (IC) which is mounted in an approximately one inch square package and is encapsulated, for example laminated, in a flexible or rigid thin film material. This material may also include a suitable adhesive backing for reliably securing the package to an outer surface or printed label of an article of interest. The IC includes therein a receiver section for driving suitable control logic and memory for decoding and storing input information such as an identification number, the baggage owner's name, point of origin, weight, size, route, destination, and the like. This memory includes, but is not limited to, PROMS, EPROMS, EEPROMS, SRAMs, DRAMs, and ferroelectric memory devices. The IC also includes a transmitter section therein operative for transmitting this information to an interrogator upon subsequent IC interrogation. An RF antenna is placed in a desired geometrical configuration (for example, monopole, dipole, loop,

bow-tie, or dual-dipole) and incorporated within or on the thin film material and adjacent to the IC in an essentially two dimensional structure, neglecting the approximately 30 mil thickness dimension of the completed structure.

Please replace the paragraph at Col. 3, lines 7-14, with the following:

In a preferred embodiment of the invention, the integrated circuit receiver and transmitter arc operated in a spread spectrum mode and in the frequency range of 200 MHz to 10 GHz, with the range of 800 MHz to 8 GHz being the range of most importance. This operation has the effect of avoiding errors or improper operation due to extraneous signal sources and other sources of interference, multipathing, and reflected radiation from the surrounding environment.

Please replace the paragraph at Col. 5, lines 48-50 with the following:

FIG. 7 is a cross-sectional view showing an arrangement of battery and capacitor alternate to the embodiment shown in FIG. 5.

Please replace the paragraph at Col. 6, lines 51-57, with the following:

FIG. 1B is a functional block diagram of an alternate enclosed transceiver of the present invention. Like numbered elements correspond to elements already described with reference to FIG. 1A. Enclosed transceiver 18 includes loop antenna 19, battery 20, and integrated circuit 21. Loop antenna 19 provides near omnidirectional communication capability as will be discussed with

reference to FIG. 11.

Please replace the paragraph at Col. 8, lines 9-26, with the following:

FIG. 3 is a plan view showing the conductive patterns on the base and cover members used in FIG. 2, including dotted line outlines of the locations for the IC and batteries. During the initial manufacturing stage for the enclosed transceiver, base 30 and cover 42 are joined at an intersecting line 44. Dipole antenna strips 34 and 36 arc shown positioned on each side of IC 32. Two conductive strips 46 and 48 serve to connect the bottoms of batteries 38 and 40 to IC 32. Conductive strip 50 is provided on the upwardly facing inside surface of top cover 42, so that, when cover 42 is folded at intersecting line 44, the outer boundary 52 of cover 42 is ready to be scaled with the outer boundary 54 of base support member 30. Simultaneously, conductive strip 50 bonded by the conductive epoxy to batteries 38 and 40, completes the series electrical connection used to connect batteries 38 and 40 in series with each other and further in series circuit with integrated circuit 32 through conductive strips 46 and 48.

Please replace the paragraph at Col. 9, lines 11-25, with the following:

FIG. 6A through FIG. 6E are cross sectional views taken along lines 6-6 of FIG. 5 showing five processing steps used in constructing the embodiment shown in FIG. 5. Base starting material includes a first or base polymer layer 78, such as polyester or polyethylene, which is laminated with a relatively impermeable material such as metal film, PVDC, or silicon nitride. Base layer 78 is coated on the bottom surface thereof with a suitable adhesive

film 80 which will be used for the device adhesion during device usage. If the adhesive is sufficiently impermeable, the impermeable coating may be omitted. The battery connection and attachment are made on the upper surface of base layer 78 using a spot of conductive epoxy. Conductive epoxy is also used at interface 94 between battery 60 and capacitor 62 and interface 98 between capacitor 62 and 1C 64.

Please replace the paragraph at Col. 9, lines 41-50, with the following:

Referring now to FIG 6C, prefabricated insulating layer 100 is now laid over the battery/capacitor/IC stack in the geometry shown. Layer 100 includes openings 102, 104, 110, and 112 therein for receiving a conductive polymer material as will be described below in the following stage of the process. Prefabricated holes 102, 104, 110, and 112 in layer 100 are aligned, respectively, to the battery contact, to the capacitor contact, and to the contacts on the top of IC 96. Layer 100 is then scaled to base polymer layer 78 using, for example, a conventional heating or adhesive step.

Please replace the paragraph at Col. 10, lines 6-27 with the following:

FIG 7 is a cross-sectional view showing an arrangement of battery and capacitor alternate to the embodiment shown in FIG. 5. As shown in FIG. 7, the battery and capacitor are mounted side-by-side under the IC. The electrical connection for battery 118 and capacitor 120 to integrated circuit 96 is provided by positioning the battery 118 and capacitor 120 in the co-planar configuration shown on the surface of base polymer layer 78. The bottom plate of battery 118 is connected through conductive epoxy layer 128 to the

top surface of IC 96. The bottom plate of parallel plate capacitor 120, is connected through conductive epoxy layer 128 to the top surface of the IC 96. A small space 126 is provided as shown to electrically isolate battery 118 and capacitor 120. In addition, in this embodiment of the invention, conductive material 128 is extended as shown between the left side opening 130 in the layer 100 and a lower opening 132 in layer 100. In a manner similar to that described above with reference to FIGS. 6A through 6E, layer 114 is then extended over the top surface of layer 100 in the geometry shown. Conductive polymer material 128 extends to connect the crossed antenna structure of FIG. 5 to IC 96 shown in FIG. 7.

Please replace the paragraph at Col. 12, lines 23-44, with the following:

FIG. 12 is a cross-sectional view taken along lines 12--12 of FIG. 11 showing a portion of the web shown in FIG 10 and illustrating electrical coupling to and between the films. The completed assembly includes similarly numbered elements already discussed with reference to FIG. 11. IC 290 is prepared for assembly by forming conductive bumps 306 and 314 to terminals on its lower surface. In a preferred embodiment, bumps are formed of conductive epoxy. In an alternate embodiment, metallic bumps, such as gold, are formed by conventional integrated circuit processes. IC 290 as shown is in a "flip chip" packaging orientation having substantially all circuitry formed on the surface facing film 230. Prior to assembly, a puddle of conductive epoxy is applied to contacts 250 and 242. IC 290 is then located atop contacts 250 and 242 so that bumps 306 and 314 are surrounded within puddles 302 and 310. The film is then heated to set all conductive epoxy including puddles 302 and 310, as well as strips and areas including the

antenna and contact areas 226 and 254, formed of conductive epoxy. Finally, top film 214 is aligned over bottom film 230 so that contact areas 226 and 254 are pressed together.

Please replace the paragraph beginning at Col. 12, line 58, and ending at Col. 13, line 11, with the following:

In the first step 410, barrier material, such as a silicon nitride deposit, is formed on the outer surface by sputtering, or by chemical vapor deposition (CVD), preferably plasma enhanced CVD. The deposit provides a hermetic barrier to prevent water vapor and other contaminants from affecting (e.g. oxidizing) battery and transceiver components. In a first embodiment the resulting thickness of the deposit is from 400 to 10,000 angstroms. In another embodiment, where thin deposits are desirable, coating on both sides of the film prevents pin holes in each deposit from aligning in a way that defeats hermeticity. The thickness of the deposit and the manner of formation arc design choices based on the selection of materials for the film and the deposit, as well as the system requirements for hermeticity over time. For example an alternate and equivalent embodiment uses other barrier materials including silicon oxide and silicon nitride deposited at a thickness of 100 to 400 angstroms. The barrier material is formed in such an embodiment using one of the processes including evaporation deposition, chemical vapor deposition, and plasma-enhanced chemical vapor deposition.

Please replace the paragraph at Col. 13, lines 32-44, with the following:

In step 430, conductors are screen printed onto the films. In a preferred embodiment, the conductors are formed on top of

laminate adhesive. Areas such as grid conductors 222 and 238 shown in FIG. 11 for contacting the battery arc, consequently, interspersed with areas of exposed laminate adhesive to provide a more durable enclosure. In this embodiment, a polymer thick film ink is employed. High conductivity is provided by such inks that include copper or silver constituents. The ink preferably provides a stable surface for electrical butt contact formations. A low oxidation rate at storage temperature is desirable, though oxidation could be minimal in a controlled manufacturing environment.

Please amend the full paragraph at Col. 13, line 52, as follows:

Third, a single conductor in the top layer accomplishes both the first and second functions. See, for example, the conductor in FIG. 11 identified as areas 226, 222, and [216] 218.

Please replace the paragraph at Col. 14, lines 16-25, with the following:

In stop 480, integrated circuit die are placed so that epoxy bumps previously formed on the integrated circuit enter the puddles formed in step 470. The arrangement of the integrated circuit face down on the bottom film is commonly referred to as "flip-chip" orientation. In an alternate and equivalent embodiment, integrated circuits are also placed in contact puddles formed on the top, i.e. cover layer. All die on the sheet are placed and aligned in this stop 480 prior to proceeding with subsequent cure.

Please replace the paragraph at Col. 14, lines 33-37, with the following:

In stop 500, an encapsulation material, commonly called "glob top epoxy" is applied over the integrated circuit. Suitable nonconductive materials include those providing a stiffening property to protect the integrated circuit and the electrical connections thereto from mechanical damage.

Please replace the paragraph at Col. 14, lines 58-61, with the following:

In step 540, the top cover film is pressed onto the bottom base film and heat is applied to activate the adhesive applied in step 420. For butyl acrylate adhesive a temperature of from 95 to 110 degrees Celsius is preferred.

Please replace the paragraph at Col. 16, lines 4-22, with the following:

Various modifications may be made in and to the above described embodiments without departing from the spirit and scope of this invention. For example, various modifications and changes may be made in the antenna configurations, battery arrangements (such as battery stacking), device materials, device fabrication steps, and the functional block diagrams without departing from the scope of this invention. The various off-chip components such as the antenna, battery, and capacitor are manufactured on-chip in alternate and equivalent embodiments. As a second example, the antenna in another alternate and equivalent embodiment is formed on the outer surface or within the outer film. In such an arrangement, coupling to the antenna is through the capacitance of the outer film as a dielectric. When formed on the exterior, the material comprising the antenna also provides hermeticity to the film for protecting the enclosed transceiver. Accordingly, these and

equivalent structural modifications are within the scope of the following appended claims.